

## PATENT ABSTRACTS OF JAPAN

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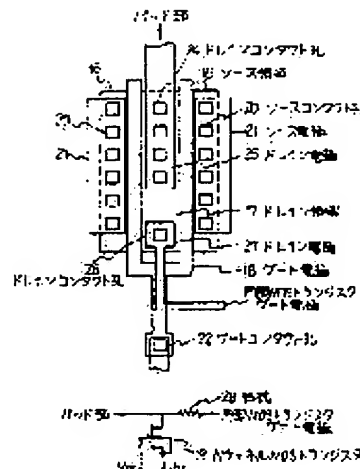
(21) Application number : 02-222922 (71) Applicant : NEC CORP  
 (22) Date of filing : 24.08.1990 (72) Inventor : FUTAMI HARUJI

## (54) SEMICONDUCTOR INTEGRATED CIRCUIT

## (57) Abstract:

PURPOSE: To eliminate the need of a protective resistance composed of a polycrystalline silicon layer so as to reduce the layout area of a whole protective circuit by utilizing the resistance component of the drain area of a MOS transistor used as a protective element as the protective resistance.

CONSTITUTION: In this semiconductor integrated circuit provided with a protective element 19 connected between a pad section for connecting an external circuit and an internal circuit, a gate electrode 18 and source area 16 connected to the power supply wiring VSS to the highest or lowest potential of the internal circuit, the first drain electrode 25 which is provided at one end of the a drain area 17 and connected to the above-mentioned pad section, and the second drain electrode 27 which is proved at the other end of the area 17 and connected to the gate electrode of the MOS transistor of the internal circuit are provided. For example, an N-channel MOS transistor 19 is used as a protective diode and the resistance component 28 in the drain area 17 between the contact hole 24 of the first drain electrode 25 and the contact hole 26 of the second drain electrode 27 is used as a protective resistance for constituting a protective circuit.



## LEGAL STATUS

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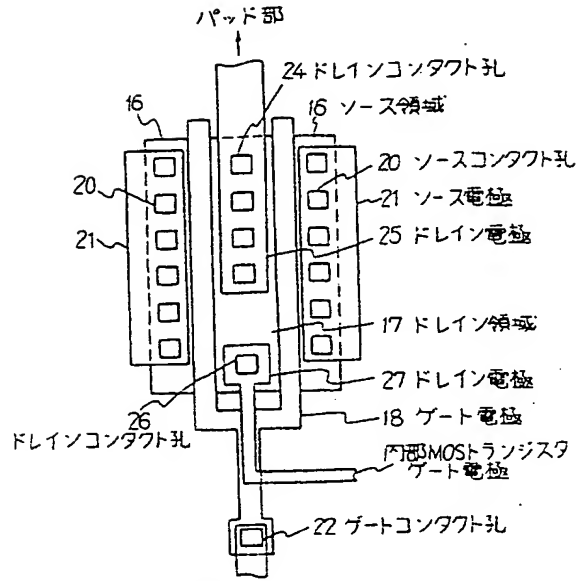




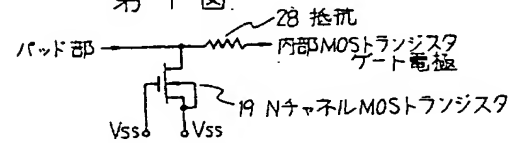
集積回路の第1の例を示すレイアウト図及び等価回路図、第7図及び第8図は従来の半導体集積回路の第2の例を示すレイアウト図及び等価回路図である。

1, 2...保護抵抗、3, 4...保護ダイオード、5, 16...ソース領域、6, 17...ドレイン領域、7, 18...ゲート電極、8, 20...コンタクト孔、9, 21...ソース電極、10...コンタクト孔、11...ドレイン電極、12, 22...コンタクト孔、13, 19...NチャネルMOSトランジスタ、14...保護抵抗、23...ゲート電極、24...コンタクト孔、25...ドレイン電極、26...コンタクト孔、27...ドレイン電極、28...抵抗。

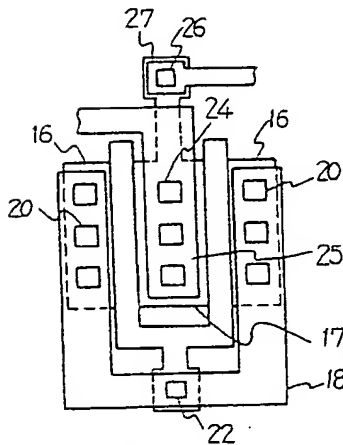
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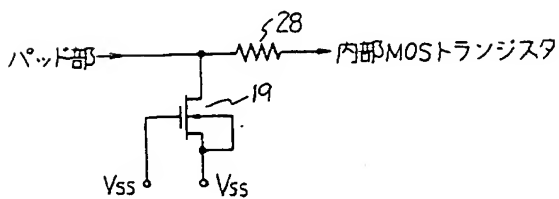
第1図



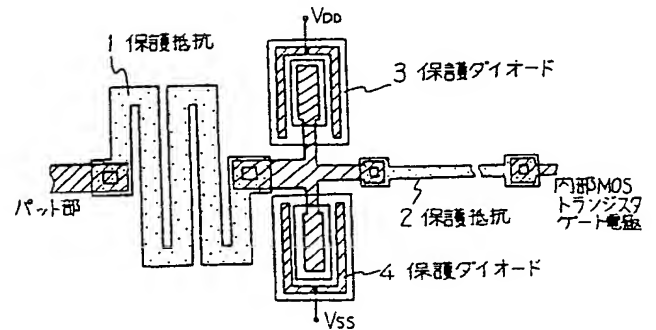
第2図



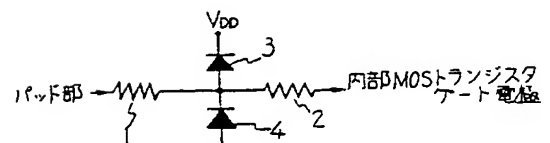
第3図



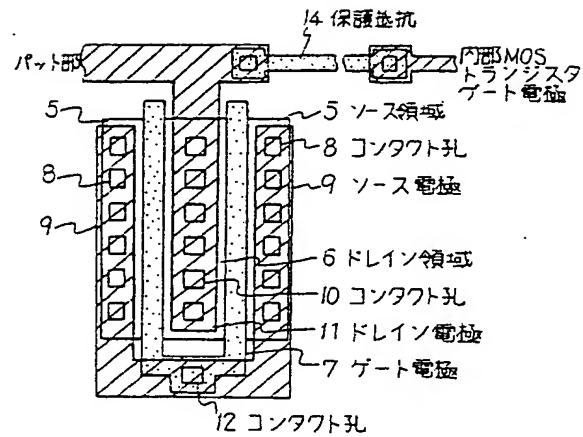
第4図



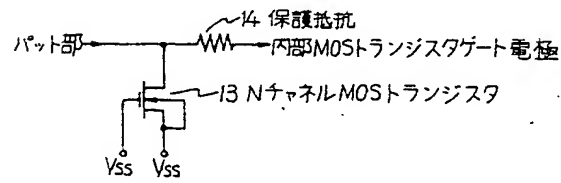
第5図



第6図



第 7 図



第 8 図